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10/589,586

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Masatoshi Nakanishi

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EXAMINER

LEGESSE, HENOK D

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/589,586	Applicant(s) NAKANISHI ET AL.	
	Examiner HENOK LEGESSE	Art Unit 2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 January 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input checked="" type="checkbox"/> Other: <u>1 Foreign reference (JP 2001-162849)</u> |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1,2,4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiyouji Noriyoshi (JP pub# 2001-162849) in view of Itoh (US 5,786,839).

Regarding claim 1, Shiyouji teaches a thermal printhead (fig.1; top view of thermal head) comprising:

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a plurality of heating resistance sections (heating elements, 2 in fig.1) arranged on a substrate (1) side by side in a primary scanning direction (see fig.1);

a common wiring portion (common electrode, 4 in fig.1) at least part of which extends in the primary scanning direction (see fig.1) while being spaced from the heating resistance sections (2) in a secondary scanning direction (see fig.1);

a plurality of first lead wiring portions (individual lead electrodes, 3 in fig.1 which are connected to 4) each including a first end connected to the common wiring portion (4) and a second end connected to a respective one of the heating resistance sections (2) (see fig.1); and

a plurality of second lead wiring portions (individual lead electrodes, 3 in fig.1 which are connected to driver IC 6) extending from the heating resistance section (2) toward the common wiring portion (4) for connecting the heating resistance sections (2) to a drive IC (6) (paragraph 0002);

wherein the common wiring portion (4) is segmented into a plurality of blocks arranged side by side in the primary scanning direction (from fig.1 it is clear that each block which is defined between voltage feed electrodes 8 and driver IC 6, repeats side by side in the primary scanning direction), and voltage is applied to opposite ends of each of the blocks in the primary scanning direction (voltage is applied through voltage feed electrodes 8); and

wherein the plurality of heating resistance sections (2) are segmented into a plurality of other blocks (see fig.1; heating elements 2 corresponding to on

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driver IC defines a block of 2) corresponding to the blocks of the common wiring portion (4), and, in each of said other blocks, resistance of the heating resistance sections (2) reduces as proceeding from opposite ends toward center of the block in the primary scanning direction (in this case as proceeding from opposite ends of external connection terminals of common electrode 4 ,i.e. from terminals 8, to wards the center of the block, the resistance value of the heating resistors 2 decreases. See the abstract and paragraph 0012).

Shiyouji does not teach wherein the first ends of those first lead wiring portions (individual lead electrodes, 3 in fig.1 which are connected to 4) connected to each block of the common wiring portion (4) are spaced from each other by a smaller distance than a spacing between the second ends of those first lead wiring portions (individual lead electrodes, 3 in fig.1 which are connected to 4) connected to each block of heating resistance sections (2).

However, from the same endeavor Itoh teaches lead wiring portions arranged such that the first ends (i.e. the ends of leads 10 where the leads are connected to the common wiring portion 13) of the first lead wiring portions (10 in figs.4A, 5A, 6,16,21; as clearly shown in the figures especially in fig.6, the lead wirings 10 are connected to common wiring 13) connected to each block of the common wiring portion (13, see fig.6,4A,5A) are spaced from each other by a smaller distance than a spacing between the second ends (i.e. the ends where the leads are connected to the heating resistance sections) of those first lead wiring portions connected to each block of heating resistance sections (5 in figs.4A,5A, R in fig.6) (Note that the lead wiring portions arrangement of both

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lead wirings 10 and 11 in figs.4A,5A,16, and 21 is the same/similar in that the wiring leads 10/11 in each block converges to wards each driver IC 8/corresponding wiring portions 13,12, and the wiring leads 10/11 diverge as they approaches each block of resistance sections 5).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to arrange the lead wirings of Shiyouji such that the wiring leads converges going towards each block of common wirings portions/driver IC and diverges going towards the resistance sections based on the teachings of Itoh. The motivation being such arrangement of lead wirings allows to connect a very small/compact drive IC to a longer/bigger array/block of heating resistances (e.g. to utilize a driver IC having half the size of driver IC of Shiyouji). This reduces the over all size of the printhead.

Regarding claim 2, Shiyouji further teaches the plurality of first lead wiring portions (individual lead electrodes, 3 in fig.1 which are connected to 4) are generally equal to each other in resistance (paragraph 0012, lines 1-2, also see fig.1), and the plurality of second lead wiring portions (individual lead electrodes, 3 in fig.1 which are connected to driver IC 6) are generally equal to each other in resistance (paragraph 0012, lines 1-2, also see fig.1).

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Regarding claim 4, Shiyouji further teaches a plurality of drive ICs (driver IC 6 in fig.1) are provided, and each of the drive ICs (6) corresponds to a respective one of said other blocks of the heating resistance sections (2).

Regarding claim 5, Shiyouji further teaches a plurality of third lead wiring portions (see fig.1; U character-like wirings above each pairs of heating elements 2) each connecting adjacent pair of the heating resistance sections (2) arranged in the primary scanning direction;

wherein the drive IC (6) is arranged closer to the common wiring portion (4) than to the heating resistance sections (2) in the secondary scanning direction; and

wherein the first lead wiring portions (individual lead electrodes, 3 in fig.1 which are connected to 4) and the second lead wiring portions (individual lead electrodes, 3 in fig.1 which are connected to driver IC 6) are alternately arranged in the primary scanning direction to be connected to respective pairs of the heating resistance sections (2) and extend from the heating resistance sections (2) toward the common wiring portion (4).

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiyouji in as modified by Itoh above and further view of Yasuda (US 6,612,672).

Regarding claim 3, Shiyouji substantially teaches the claimed invention, see paragraph 0013 and the rejection of claim 1 above, but failed to expressly

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teach the first lead wiring portions (individual lead electrodes, 3 in fig.1 which are connected to 4) are unequal in length, and the second lead wiring portions (individual lead electrodes, 3 in fig.1 which are connected to driver IC 6) are unequal in length, wherein a longer one of the lead wiring portions has a larger width at least partially.

However, from the same endeavor Yasuda teaches wirings that connect heating elements to a power sources arranged such that the wirings are unequal in length. The shortest wire (the wire nearest to the power supply side in fig.6) is formed smallest in width and the longest wire (the wire furthest from the power supply side in fig.6) is formed largest in width in order to ensure the resistance of the wires running to different heating elements are equal (fig.6; col.8, lines 18-33).

Therefore it would have been obvious to one having ordinary Skill in the art at the time the invention was made to form the first and second lead wiring portions of Shiyouji made unequal in length, wherein the longer one of the lead wiring portions has a larger width based on the teachings of Yasuda. The motivation is to ensure the resistance of the wires used for connecting the heating elements uniform, thereby realizing a uniform supply of current to each of heating elements which results in better print image quality (col.8, lines 18-33 of Yasuda).

Response to Arguments

5. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HENOK LEGESSE whose telephone number is (571)270-1615. The examiner can normally be reached on Mon - FRI, 7:30-5:00, ALT.FRI EST.TIME.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Luu can be reached on (571) 272-7663. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

H.L.
05/13/2008

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Supervisory Patent Examiner, Art
Unit 2861